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Abstracts

II.



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A dual way of computing - learning from cerebral asymmetry

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Extended summary

Despite the impressive technical and conceptual power of digital/logical computing there has been signes and facts showing its inherent practical and theoretical barriers. Computing structures using artificial electronic copies of a yet oversimplified but analog regular model of biological neuron (instead of the more primitive yes-no logical model) demonstrated striking capabilities in some examples. These types of artificial analog/"neural" circuits or "neural" computing provided an alternative regular analog solution for some problems which resisted the attacks of the digital/logical way of problem-solving of artificial intelligence, although a lot of important questions are open.

Hence, we have <u>two types of computing</u> (processing) paradigms, the digital/logical and the analog/"neural" way which offer different capabilities. In both cases the strong underlying facts are the different models of the biological neuron operations.

In course of learning from the nature to provide better artificial (electronic) information processing systems it has been recently realized by the author that facts and analogies concerning the functional cerebral asymmetry could strongly motivate the introduction of a <u>dual way of computing</u> structure¹. It is emphasized immediately that it is not the modelling of the cerebral functions, it is simply a one way street from cerebral asymmetry² to electronic computing using some facts concerning the qualitative features of nonlinear circuits and operators^{1,4,5} and motivated also by the unified view of physical-information-and circuit-aspects of information processing³. The aim of this paper is to introduce the dual computing structure in a less technicalmathematical framework.

The <u>basic motivating facts</u> and results are as follows. A. Cerebral asymmetry $2^{2,6,8}$

(i) A representative sample of the different functional processing abilities of the left and right hemispheres (LH-RH) are summarized next (selected for our purposes)

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- \mathbf{LH}
- analytic (breaking into parts)
- differential
- sequential processing and temporal resolution of information
- verbal abilities
- matching of conceptually similar objects
- isolate a "shape" in irrelevant background (a surprise in LH performance)
- information ordered in time
- events of high rate of change (< 50 msec)

- RH
- holistic (global)
- integral
- immediate processing and perception of the parts vs. whole relation
- performing abilities
- matching of structurally (pictures, curves etc) similar objects
- forming whole "gestalt" from incomplete information
- information ordered in space
- events of small rate of change

(ii) The dual memory encoding hypothesis in memory theory says that verbal (name) an pictorial symbols of a notion is represented parallel (a special dual representation is the metaphore). (iii) Simultaneous processing in some tasks²,⁶ (e.g.

(e.q. expert musicians realizing melody and structure jointly).

(iv) Direct (real time) realization and detection of complex inputs (e.g. the "grandmother cells").

(v) The competency level of a given hemisphere for some particular task, i.e. the division of labour between the hemispheres is changing depending on attentional focusing and other factors.

other factors°. (vi) Many neurons are organized in a few layers of two dimensional arrays containing modules which are columns of this organization and these modules have specific functions.

B. Nonlinear circuits and systems

(i) Any n-variable function can be realized by a three layer structure of one variable nonlinear transfer function elements. (ii) Any nonlinear operator is unique except scaling and delay 3.

(iii) An operator with fading memory can be approximated by a nonlinear memoryless operator and delays in a forward structure

(iv) Cellular neural networks are able to consider local and global information processing on a finite 2- or 3-dimensional analog processor grid

The notion of the analog event is important. It is a continuous signal on a finite time segment with some specific storing and processing properties¹. The digital events are the verbal symbols coded in a 0-1 fashion.

Now, we summarize the dual computing structure. It conists of five main parts including different computing modules.



(i) the memory encoding part (Me)
(ii) the dual (digital and analog) memory (M),
(iii) the digital controller (C)
(iv) the processing arrays (Pa)
(v) the memory decoding part (Md)

controller (C) is a standard digital finite state machine The with an inherent finite memory making unique digital-logical decisions (next state functions and output functions). The memory (M) has a dual structure, a digital and an analog part. All the other three parts have basically three building blocks, the three processors: (i) the digital/logical (for the verbal hemisphere analogy), (ii) the analog/"neural" (for the non-verbal hemisphere analogy) and (iii) a joint processor-pair having the preceding two processors with internal feedback. In this model the application of the analog-events provides real-time, "immediate" detection of some prescribed patterns (templates). The digital processor array is a 1-, 2- or 3-dimensional array of simple digital processors working in systolic/cellular mode (communicating with strict neighbours only) or in connection mode (all processors communicate with all others). The analog processor array is again a 1-, 2- or 3-dimensional array of analog processors (nonlinear amplifiers) connected through weighted paths (feedback or feedforward by e.g. resistors). In the cellular neural networks⁷ connection is in a finite processor-distance neighbourhood. The crucial element of the dual computing structure is the joint processor shown below.





The crucial parts are the two feedback paths: the logical analog "neural" (l/n) and the analog "neural" - logical (n/1) paths. The l/n path controls the elements of the T and P matrices of the feedback modules (or the weight parameters of the forward modules). The n/l path controls the memory contents of the logical/digital processor performing the recursive functions. Hence, (i) a mutual coupling is introduced between the recursive functions and the algorithmic elements of the neural circuits (extended recursive functions), (ii) real-time detection of standard but complex events, (iii) logical control of dynamic properties of "neural" processors and (iv) dynamic control of logical inference sequences of the logical processors.

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